SEANet G2: Toward a High-Data-Rate Software-Defined Underwater Acoustic Networking Platform

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ABSTRACT

Existing underwater acoustic networking platforms are for the most part based on inflexible hardware and software architectures that can support mostly point-to-point, low-data-rate, delay-tolerant applications. Most commercial devices do not provide neither the sufficient data rates nor the necessary flexibility to support future underwater networking applications and systems. This article discusses a new high-data rate software-defined underwater acoustic networking platform, SEANet G2, able to support higher data rates (megabit/s data rates are foreseen over short range links), spectrum agility, and hardware/software flexibility in support of distributed networked monitoring operations. The article reports on the main architectural choices of the new platform, as well as some preliminary performance evaluation results. Data rates in the order of megabit/s were demonstrated in a controlled lab environment, and, for the first time to the best of our knowledge, data rates of $522\,\mathbf{kbit/s}$ where obtained in sea trials over short horizontal links (e.g., $10\,\mathbf{m}$) for a BER lower than 10^{-3}.

Keywords

Underwater Acoustic Networks, Software-Defined Networks, Underwater Modems

1. INTRODUCTION

Underwater acoustic networking technology plays a key role in many commercial, scientific, and military activities at sea. In the last few years, there have been significant efforts to advance underwater networked sensing, communication, and control systems to develop new solutions to many

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pressing problems of our times, including (i) climate change monitoring, pollution control and tracking; (ii) providing sophisticated control systems for the oil and gas industry; (iii) disaster prevention; (iv) tactical surveillance.

In spite of increased attention, current underwater acoustic wireless communication platforms are still based on inflexible hardware that can support mostly point-to-point, low-data-rate, and delay-tolerant applications [1,2]. Regrettably, these devices do not provide the data rates or the flexibility required to enable future underwater networking applications and systems that envision i) real-time video streaming, ii) capability to control and adapt in real time communication parameters (including modulation, frequency channel, coding scheme, channel access probability) based on channel condition/state and application needs, and iii) capability to develop and test advanced networking schemes. Therefore, there is a need for new underwater acoustic networking platforms that will enable development and testing of next-generation networking schemes, as well as networked monitoring applications with fixed and mobile underwater devices.

To this end, in this paper we propose and discuss the design of a new high-data rate software-defined underwater acoustic networking platform, SEANet G2 (2nd Generation), with characteristics in terms of data rate (megabit/s data rates are foreseen over short range links), spectrum agility, and hardware/software flexibility in support of distributed networked monitoring operations.

SEANET G2 is envisioned to provide several benefits over existing underwater acoustic platforms:

- **Megabit/s Data Rates.** SEANet G2 is designed to achieve data rates at least one order of magnitude higher than state of the art commercial devices over short and moderate range links. Data rates of 522kbit/s were achieved over short links (e.g. $10\,\mathrm{m}$) for a bit-error-rate (BER) lower than 10^{-3}; megabit/s data rates were demonstrated in a controlled lab environment; megabit/s data rates over short-range links (e.g., $50-100\,\mathrm{m}$ in the $0-2\,\mathrm{MHz}$ acoustic spectrum) are foreseen with appropriate acoustic front ends for the proposed platforms.

- **Spectrum Agility - Cognitive Capabilities.** SEANet G2 is able to switch operational frequency at run time, with purely software-defined adaptation, to operate over different spectrum bands, with varying width and spectral signature.

- **Physical Layer Reconfiguration.** SEANet G2's

physical layer is implemented on a reconfigurable FPGA, and can be reprogrammed at runtime (reconfiguring parameters such as modulation, coding, and power, as well as switching between different physical layer schemes altogether).

- **Cross-layer Controllable Protocol Stack.** SEANet G2's networking protocol stack is based on a fully reconfigurable architecture, where a set of pre-defined primitives will ease the design of cross-layer control strategies where both hardware (through a flexible FPGA) and a software-defined networking protocol stack are jointly controlled to adapt to the time-varying state of the channel, of the network topology, and of the network traffic, thus enabling experimentation with advanced networking functionalities tightly integrated with the physical layer.

- **Integration with the Internet.** SEANet G2 hosts a Linux operating system, natively able to run Internet-based applications and network monitoring tools. An adaptation layer [3] provides integration with the Linux IP Stack.

- **Wireless Recharging Capabilities.** SEANet G2 has the capability of harvesting power to recharge batteries from acoustic links, thus providing higher flexibility in deployment.

In this paper, specifically, we report on the early stages of the design of the hardware, software, and network architecture of the SEANet G2 platform. Moreover, we demonstrate data rates of 522 kbit/s achieved at sea over short horizontal links (i.e., 10 m) for a BER lower than 10^{-3}. We also showcase data rates in the order of megabit/s in a controlled lab environment.

The remainder of this article is organized as follows. In Section 2, we briefly review related work. Then in Section 3, we present the architecture of the SEANet G2 platform. In Section 4, we introduce the SEANet G2 prototype while in Section 5 we present performance evaluation results. Finally, we draw conclusions in Section 6.

2. RELATED WORK

Most existing commercial modems were designed to provide low-rate connectivity over long ranges (i.e., in the order of at least 1 km). Since attenuation in underwater channels increases exponentially with frequency [2], to achieve long ranges most modems operate over relatively low frequency bands. Commercial modems often provide waveforms that achieve data rates around 20 kbit/s with a link distance of 1 km over horizontal links [1, 2]. For example, Teledyne Benthos [4], a leading manufacturer of underwater acoustic equipment in the United States, offers a wide range of acoustic modems that operates over a 5kHz acoustic band between $8 - 13$ kHz with proprietary PSK and MFSK transmission schemes that can support data rates up to 15 kbit/s over $(2 - 6$ km) underwater links. AquaSent AM-OFDM-13A [5] is another commercial underwater acoustic modem that can communicate at a range 5 km with a maximum data rate of 9 kbit/s. Other commercial modems, such as the Evologics 52CMHS [6], can reach data rates of 62.5 kbit/s over a range of 300 m. Overall, while commercial modems can support some existing underwater applications adequately,

they are not suitable for many potential new sensing and control applications (for example in support of the oil and gas and fishing industries) that require higher data rates over shorter distances. Moreover, commercial modems are typically based on fixed hardware solutions that incorporate proprietary protocols. As a result, they do not offer adaptation capabilities, which limits the capabilities of underwater networks and applications in *temporally* and *spatially* variable underwater channel conditions. To overcome this limitation, several papers [7–10] have focused on adaptive physical layer schemes, mostly proposing techniques to switch among a small number of operational modes offered by commercial modems. Therefore, they may satisfy the requirements of specific application scenarios, while they are still lacking the capability of real-time reconfiguration beyond a limited number of operational modes.

Considering the limitations of commercial modems, there have been research efforts focused on developing new modems that offer support for adaptation through partial or full software-defined protocol implementations. In [11], a USRP-based (a commercial software defined radio) underwater acoustic networking platform that uses open-source software tools (GNU Radio, TinyOS, and TOSSIM) to implement physical and data-link layer functionalities was presented. The platform offers parameter adaptation capabilities at the physical and MAC layers. Similarly, in [12, 13], and [14], underwater acoustic modems that are based on FPGA/DSP or FPGA-only cores were proposed. The modems were reported to provide support for software-defined physical and data-link layers that enable real-time parameter adaptation. With similar goals, in our previous work [15, 16], we proposed an underwater acoustic networking platform based on USRP with external controller on a laptop running the protocol stack and offering real-time reconfiguration capability at the physical layer. In [17], we presented a first generation SEANet platform based on pure software-processing on a resource-constrained Cortex microcontroller, which offers adaptation at multiple layers through its software-defined functionalities that span physical, data-link, network, and application layer.

In this work, we propose and discuss the architecture of a new high-data rate software-defined underwater acoustic networking platform based on a Zynq board that provides FPGA-based low-level processing functionalities as well as a more powerful CPU (with more memory) than a typical microcontroller. The combination of processor and FPGA offers hardware and software reprogrammability. The processor is responsible for executing software-defined functionalities and to define reconfigurable high-level networking protocols, i.e., non-time critical MAC functionalities, network, application. The FPGA is in charge of physical layer and time-critical MAC layer functionalities. In this way, processing-intensive physical layer functionalities are software-defined, but executed *in hardware* that can be reconfigured in real-time (through registers and partial reconfiguration of the FPGA). Therefore, unlike purely software-defined implementations that introduce high processing latency [18, 19] and limit data rates; or pure hardware implementations that lack reconfiguration capabilities, SEANet G2 is able to provide both the low latency and high-data-rate characteristics of hardware implementations, as well as the reconfiguration capabilities of software implementations.
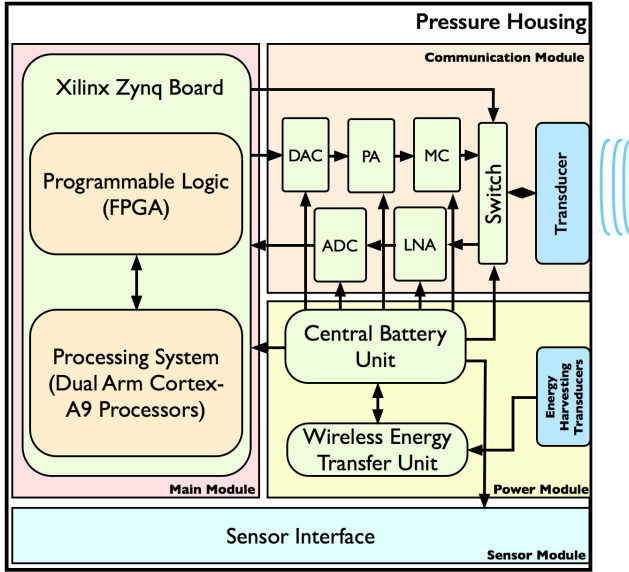
Figure 1: SEANet G2 hardware architecture.

3. SEANET G2 ARCHITECTURE

SEANet G2 is a modular hardware and software architecture that provides a basis to form high-data-rate, software-defined underwater acoustic networking devices. SEANet G2 (i) enables hardware evolution and reconfiguration; (ii) offers a modular set of libraries at the physical, data-link, network, and application layers; (iii) can provide cross-layer reconfiguration capabilities; (iv) can facilitate new protocol designs and hardware/software enhancements, through its modular architecture. In this section, we describe the details of the hardware and software architecture of the SEANet G2 platform.

3.1 Hardware Architecture

SEANet G2 has a hardware architecture with building blocks similar to the previous generation SEANet platform [17]. It is structured into four modules, i.e., main, communication, power, and sensor module, as illustrated in Fig. 1. Each module is designed to be swappable/upgradeable as it is interfaced to other modules through standard interfaces and has distinct, non-overlapping functionalities. In this way, SEANet G2 platform can provide hardware evolution and reconfiguration to adequately support different applicational needs.

The main module incorporates a field programmable gate array (FPGA) and a general purpose processing unit. The combination of processor and FPGA provides hardware and software reprogrammability. The processor is responsible for executing software-defined functionalities to define reconfigurable high-level networking protocols, i.e., non-time critical MAC functionalities, network, application. The FPGA is in charge of physical layer and time-critical MAC layer functionalities. In this way, processing-intensive physical layer functionalities are software-defined, but executed *in hardware* that can be reconfigured in real-time (through registers and partial reconfiguration on the FPGA). The communication module enables acoustic/ultrasonic wireless connec-

tivity through data converters, power/low-noise amplifiers (LNA), and an acoustic transducer. It consists of a receiver (Rx) and a transmitter (Tx) chain. The Rx chain includes a low-noise amplifier (LNA) and an analog-to-digital converter (ADC) to amplify and digital-convert received signals, while the Tx chain embeds a digital-to-analog converter (DAC) and a power amplifier (PA) to analog-convert and amplify the digital waveforms before transmission. The Tx chain also includes a matching circuitry (MC) to match the input impedance of an acoustic transducer with the output impedance of a PA to minimize the amount signal that is reflecting back to a PA and not transmitted. Moreover, the communication module incorporates an electronic switch that allows using a single acoustic transducer for both transmitting and receiving acoustic signals in a time-division fashion. The power module includes a unit that powers the SEANet G2 platform and energy harvesting transducers interfacing with a wireless energy transfer unit that enables wirelessly recharging of the central battery unit through acoustic waves. The sensor module provides an interface for several different sensors through either standard analog interfaces, e.g., ADC, or digital interfaces, e.g., Serial Peripheral Interface (SPI).

3.2 Software Architecture

SEANet G2 has a modular, evolvable, and reconfigurable software architecture, as depicted in Fig. 2. The software architecture depends on a Linux operating system running on the processing unit and communicating to the FPGA fabric using AXI interfaces. All physical layer functionalities as well as the time-critical MAC functionalities are implemented in the FPGA, while non-time critical MAC, network, and application layer functionalities are executed on the processing unit.

Physical Layer. The software architecture includes physical layer building blocks and libraries for defining different communication schemes and forward error correction (FEC) techniques. Specifically, it incorporates a Zero-Padded Orthogonal Frequency-Division-Multiplexing (ZP-OFDM) [17, 20], Binary Chirp Spread-Spectrum (B-CSS) [20, 21], and impulsive communications, as well as Reed-Solomon (RS) and Convolutional codes. Moreover, it also hosts reusable primitive building blocks, e.g., symbol mapping, Fast Fourier Transform (FFT), filters to enable fast implementation and prototyping of new physical layer protocols.

Data-Link Layer. The software architecture (currently under development) will host a set of data-link layer libraries implementing different MAC protocols, network configurations, and physical layer adaptation mechanisms. Work is undergoing to implement a Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA) [22] and ALOHA [23], as well as a set of primitive functions including retransmissions, timers, checksum-based error control, and idle listening, to enable the implementation of different MAC protocols (e.g., TDMA-based protocols such as slotted FAMA [24]). Moreover, it includes a physical layer mechanism to define algorithms to control physical layer adaptation to the underwater channel and application requirements in real-time, including modulation, FEC coding rate, guard interval size, and symbol duration.

Network Layer. The software architecture of SEANet G2 includes our libraries [3] to support IPv4 and IPv6 protocols through an adaptation layer that provides IP header
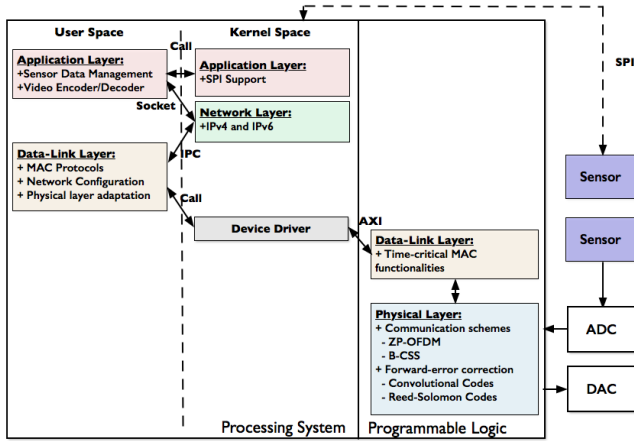
Figure 2: SEANet G2 platform software architecture.

compression, IP packet fragmentation, and optimizes the traditional IPv4 and IPv6 headers for underwater acoustic channels to minimize the overall network delay and energy consumption [3]. Moreover, it will incorporate implementation of different routing protocols including [25–27].

Application Layer. The software architecture will incorporate libraries to provide support for interfacing different sensor units, either through ADCs in the analog domain or through digital domain with standard serial communication protocols, i.e., SPI. It will also include video encoders and decoders for supporting real-time video transmission. Moreover, since it runs a Linux operating system, existing applications developed in a Linux environments can be ported to the system.

4. SEANET G2 PROTOTYPE

In this section, we introduce the first SEANet G2 prototype that is built based on the hardware and software architecture discussed in Section 3.

4.1 Hardware Implementation

Figure 3 shows the hardware implementation of the SEANet G2 prototype.

Main Module. The main module is based on a Zynq Z-7020 System on Chip architecture [28]. Zynq integrates a feature-rich dual-core ARM Cortex-A9 based processing system (PS) and 28 nm Xilinx programmable logic (PL) (i.e., a field-programmable gate array, FPGA) in a single device. The ARM Cortex-A9 CPUs are the heart of the processing system and include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces. This architecture provides the combined benefits of (i) an ARM microcontroller that can run a Linux operating system and be programmed through high-level languages (C++, Python); (ii) an FPGA to enable hardware reconfiguration (offline or runtime) in support of different physical layer protocols and other computationally-intensive data processing operations without sacrificing on energy efficiency.

The combination of ARM processor and FPGA offers hardware and software reprogrammability with compact packaging and low energy consumption. The ARM processor

is responsible for executing the high-level networking, processing, and application-specific functionalities. Zynq architectures provide low latency, high throughput, and cache-coherent communication between the programmable logic and the ARM processor cores. In this way, processing-intensive functionalities can be software-defined, while being executed *in hardware* (FPGA). This means that the prototype does not need to trade processing latency off for reconfigurability, but instead it can run functionalities with low latency and still be able to perform reconfiguration in real-time through registers and partial reconfiguration on the Zynq FPGA.

Programmable Logic. The Xilinx ZC702 Evaluation Board XC7Z020 CLG484 -1 AP, a System-On-Chip SoC based on the Xilinx Zynq-7000 All Programmable SoC, is used in the first prototype of the SEANet G2. The programmable logic has up to 53k look-up-tables (LUTs), 85k logic cells, and 220 DSP slices in a chip scale package (17×17 mm). The Zynq Board embeds an oscillator at 33.33 MHz. A set of digital signal processing (DSP) functional blocks is available to off-load computationally expensive MCU operations to the FPGA. The Zynq Board includes 4 mixed-mode clock manager (MMCM) and 4 Phase Locked Loop (PLL) that provide a variety of user-synthesizable clock frequencies, along with custom phase delays, to support multi clock domain designs.

Processing System. The processing system of Xilinx ZC702 Evaluation Board XC7Z020 CLG484 -1 AP runs Linux and is in charge of data processing and of executing software-defined functionalities to implement non-time critical MAC functionalities, network, transport and application layer functions. While the Zynq chip includes a 256 KB on-chip RAM, the Xilinx Evaluation Board also offers a 1 GB of DDR3 SDRAM and 128 Mb of Flash memory with Quad-SPI interface. Moreover, it supports a rich set of I/O peripherals, including two I2C blocks that can operate both as master and slaves, and 118 GPIO pins to enable connectivity with virtually any sensors, data converters, and memories. The processing system is connected to the programmable logic through a multilayered ARM AMBA AXI interconnect, which enables multiple simultaneous and continuous data flows.

Communication Module. The communication module enables acoustic/ultrasonic wireless connectivity through data converters, power/low-noise amplifiers, an electronic switch, and an acoustic transducer.

Data Converters. The current prototype is designed to support frequencies in the $0 - 2$ MHz acoustic spectrum. Among many commercially available DACs and ADCs, we based our current design on two small low-power data converters, i.e., TI DAC7821 [29] and MAXIM MAX1420 [30], which satisfy the sampling rate requirements of our prototype. Specifically, TI DAC7821 operates with $12-$bit parallel inputs and can support up to 10 MHz bandwidth, thanks to its sampling rate of 20.4 Msample/s. It is connected to the Zynq Evaluation Board through General Purpose Input Output (GPIO) pins, where it gets data bits, read/write enables, and clock. MAXIM MAX1420 is a $12-$bit parallel output ADC that can support up to a sampling rate of 20.4 Msample/s. It is also interfaced to the Zynq Evaluation Board through General Purpose Input Output (GPIO) pins, where it sends data bits and gets clock input. Moreover, MAXIM MAX1420 comes in small $48-$pin TQFP packages ($7x7$ mm) and operates at low supply voltage, e.g., 3.3 V,
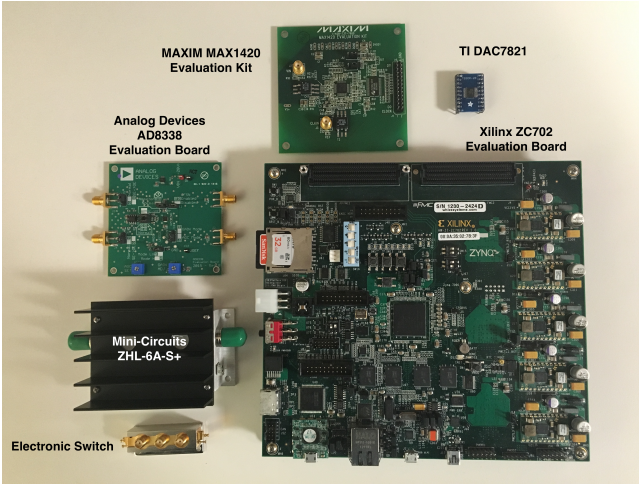
Figure 3: Hardware implementation of the first SEANet G2 prototype.

Figure 4: Wireless energy transfer unit.

while in the current prototype, an evaluation board was used.

Power/Low-Noise Amplifiers and Switch. Selecting the right amplifiers is non-trivial, since many factors need to be considered upfront, including signal bandwidth and central frequency, and characteristics of the ultrasonic transducer, i.e., sensitivity and transmission response, which affect the amplification gain requirements. The required communication range, which depends on the specific application scenario, also affects power and gain requirements. Finally, minimizing power consumption and PCB area occupancy are also major concerns. At the transmitter side, a wideband general purpose amplifier stands out as the ideal choice for use as a power amplifier due to its operating frequency range and relatively high gain level. Specifically, the Mini-Circuits ZHL-6A-S+ [31] is used, which offers a relatively high gain up to 25dB with a linear response (i.e., 34dBm IP3) up to 500MHz. At the receiver side, the low noise and low power characteristics make variable gain amplifiers (VGAs) ideal for use as receiver amplifiers. Specifically, the AD8338 [32] is used, which offers low noise figures of $4.5 \, \mathrm{nV}/\sqrt{\mathrm{Hz}}$, an operational frequency from 10kHz to 18MHz, and voltage controlled gain up to 80dB. Additionally, the AD8338 comes in small 16-lead LFCSP packages ($3x3$ mm) and operates at low supply voltage, e.g., $3-5$ V, while in the current prototype, an evaluation board was used. To allow transmitter and receiver operations with a single acoustic transducer in a time-division duplex fashion, a Mini-Circuits $ZX80-DR230+$ [31] electronic switch is employed.

Acoustic Transducer. In the current prototype, two commercial off-the-shelf (COTS) transducers were used for utilizing different parts of the spectrum. The first is the TC4013 [33] acoustic transducer (receiver hydrophone) manufactured by Teledyne RESON, which offers an operational frequency range from 1 Hz to 170 kHz. It provides receiving sensitivity of -211 [dB re 1V /μPa at 1 m] that is relatively flat over the operational frequency range and transmitting sensitivity of 130 [dB re 1μPa/V at 1 m] at 100 kHz. Moreover, the TC4013 has omnidirectional horizontal and $270°$ vertical di-

rectivity patterns.

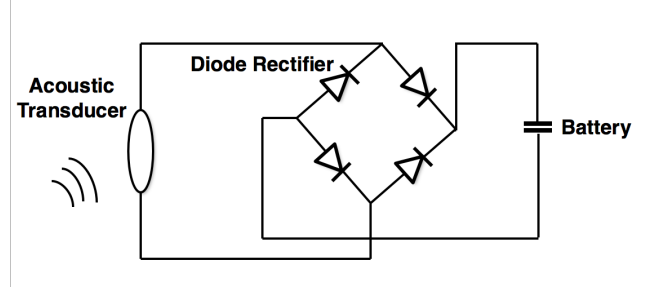The second transducer that was considered is TC4038 [33], also manufactured by Teledyne RESON. TC4038 can support an operational frequency range from 10 kHz to 800 kHz. This transducer was selected to operate over portions of the spectrum that TC4013 is not able to cover. It has receiving sensitivity of -228 [dB re 1V /μPa at 1 m] that is relatively flat over the operational frequency range and transmitting sensitivity of 138 [dB re 1μPa/V at 1 m] at 700 kHz. Moreover, TC4038 has omnidirectional horizontal and $60° - 120°$ vertical directivity patterns.

Power Module. In the current prototype, a wireless energy transfer unit that uses acoustic waves to harvest energy and recharge battery units was built and tested. The wireless energy transfer unit is based on the method know as contactless energy transfer (CET) or wireless power transmission (WPT), which is used for transmitting energy or power wirelessly and accordingly avoiding direct wired connections. Today, several WPT technologies based on different physical principles have been proposed and successfully employed. Typical approaches include inductive and capacitive WPT, which are based on electromagnetic fields (EMFs), and optical coupling [34].

Acoustic energy transfer (AET) is an innovative and still relatively underexplored methodology to transmit power remotely using acoustic/ultrasonic waves [35]. Differently form the EM waves, acoustic/ultrasonic waves need a medium to propagate and consequently transfer energy. The physical characteristics of the propagation media primarily impact the speed of the traveling wave and result in three loss effects: diffraction, attenuation and reflection [34]. Nevertheless the idea of exploiting ultrasounds as carriers of energy can be extended to underwater scenarios aiming to design a CET system immersed in water. A system for underwater WPT through acoustic/ultrasonic waves consists of three key macro components, the transmitter, the propagation medium and the receiver [35]. Different choices in the implementation of these components (including piezoelectric elements, circuitry details, choice of the operational frequency, among others) should be directed at maximizing the amount of energy transferred through water by minimizing these three types of loss.

Therefore, in the current prototype, a wireless energy transfer unit was built based on a Teledyne RESON TC4013. TC4013 is interfaced with a diode rectifier that converts the AC electrical voltage into a DC signal used to recharge a super capacitor. A schematic of the wireless energy transfer unit is depicted in Fig. 4.
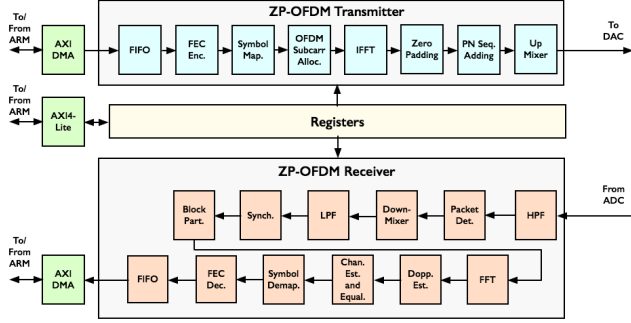
Figure 5: Block-Structure of ZP-OFDM in SEANet.

4.2 Software Implementation

SEANet G2's prototype software implementation is based on the software architecture explained in Section 3.2. The FPGA of the Zynq board hosts all physical layer implementations and time critical MAC functionalities, while the ARM processor is responsible for the implementation of the upper-layer protocols, i.e., non-time critical MAC functionalities, network layer, and application layer. In the current prototype, we implemented a ZP-OFDM scheme.

OFDM is a physical layer scheme that is specifically designed to be robust against frequency-selective channels with long delay spread [10, 17, 20, 36]. SEANet G2 includes an OFDM scheme with zero-padding, where each OFDM symbol is followed by a field including zeros. This results in improved energy-efficiency compared to other methods, e.g., cyclic-prefixing. ZP-OFDM scheme can allocate each OFDM subcarrier either as a pilot subcarrier (to be used for channel estimation and fine symbol synchronization), as a null subcarrier (to be leveraged in Doppler scale estimation), or as a data subcarrier (used for data transmission and conventionally modulated with, e.g., M-Phase-Shift-Keying (PSK) or M-Quadrature-Amplitude-Modulation (QAM)). The implemented ZP-OFDM defines a packet format where N OFDM symbols are preceded by a preamble packet that is used for packet detection and coarse time synchronization. The implemented ZP-OFDM includes two types of preamble blocks, i.e., pseudo-noise (PN)-sequence and chirp.

FPGA Design. The FPGA top-module instantiates ZP-OFDM transmitter and receiver blocks, registers, AXI4-Lite interface, and AXI DMA.

Transmitter Chain. Figure 5 depicts a block-level representation of the FPGA logic that implements the proposed ZP-OFDM transmitter. Information bits are received from the ARM processor through AXI DMA to the input FIFO of the transmitter chain. The input information bits are encoded by a Forward-Error-Correction (FEC) encoder (i.e., convolutional encoder) and later mapped into symbols according to the selected modulation scheme. The generated symbols are then allocated to different subcarriers alongside with pilot and null subcarriers based on a predefined scheme to form the OFDM symbols. The formed OFDM symbols are then forwarded to the IFFT block to be translated to the time-domain. The output of the IFFT block is then fed to the zero-padding block for generating ZP-OFDM symbols. The formed ZP-OFDM symbols are later translated into a packet format, which includes a preamble (PN sequence) and N ZP-OFDM symbols. The generated packets are later up-converted to the passband frequency by the up-mixer block and sent to the DAC for being converted to the analog domain and transmitted.

Receiver Chain. The block-level schematic off the FPGA logic implementing ZP-OFDM receiver is shown in Fig. 5. The received signals from the ADC are first fed into a high-pass filter (LPF) to eliminate DC offset and out-of-band noise. The filtered signals are then processed by a packet detector module, which is performing an energy-level collection based method for packet detection. The detected packets are later down-converted into the baseband signals through a down-mixer block. The baseband signals are then filtered by a low-pass filter (LPF) to eliminate higher frequency harmonics. Then, the correlation properties of the PN sequence in the transmitted packet are leveraged to obtain coarse time(packet) synchronization. Following the packet synchronization, each ZP-OFDM packet is then portioned into individual OFDM symbols. After taking the FFT of each OFDM symbol and translating them into the frequency domain, each OFDM symbol is passed through the blocks performing Doppler scale estimation and compensation based on pilot and null subcarriers, pilot-tone based channel estimation, zero-forcing(ZF) channel equalization, symbol detection. The detected symbols are later translated into the bits and decoded with the FEC decoder. Finally, the acquired bits are transferred to the FIFO for being send to the ARM processor through AXI DMA.

Registers. Registers are responsible for storing and reconfiguring the physical layer configuration parameters written by the ARM processor through the AXI4-Lite interface. Thanks to these registers, the physical layer configuration parameters can be reconfigured in real-time. The current implementation of the prototype allows several parameters to be reconfigured in real-time, e.g., modulation, coding rate, guard time, subcarrier mapping, number of ZP-OFDM symbols in a packet.

ARM Design. The current implementation of the prototype is based on PetaLinux operating system. It currently incorporates two main modules. The first module controls the real-time reconfiguration of physical layer configuration parameters through the AXI4-Lite interface and registers, while the second one sends and receives information bits from the physical layer through AXI DMA.
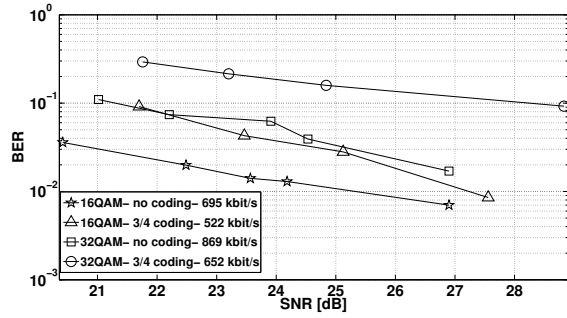
5. PERFORMANCE EVALUATION

In this section, we present three different sets of experiments that were conducted in a water test tank and at sea to conduct a preliminary assessment of the capabilities of SEANET G2. The first two sets of experiments investigate the data rate and BER performance of the SEANet G2 OFDM physical layer scheme, while the last experiment observes the capabilities of the wireless energy transfer unit.

Tank Experiments. We conducted a series of experiments in a water test tank of dimensions $228.6\text{cm} \times 55.9\text{cm} \times 73.7$ cm. Specifically, we used ZP-OFDM signals that occupy a bandwidth of $B = 600\,\text{kHz}$. We selected a carrier frequency of $f_c = 500$ kHz, to reach the highest transmit power of the prototype based on the characteristics of the acoustic transducer and amplifiers. We introduced guard intervals of 14.5 ms for each OFDM block.

In the experiments, we specifically concentrated on the
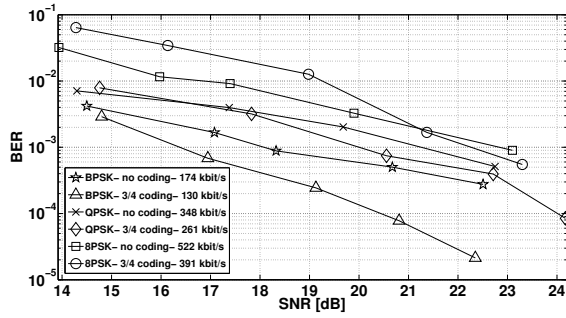
(a) BPSK, QPSK, and 8PSK with or without coding. (b) 16QAM and 32QAM with or without coding.

Figure 6: BER versus SNR for different modulations with or without $3/4$ convolutional coding.

Modulation	BER	SINR [dB]	Data Rate [kbit/s]
BPSK	1.80*10-3	29.52	308
QPSK	4.10*10-3	28.42	617
8PSK	1.08*10-2	29.83	926
16QAM	4.67*10-2	30.08	1234
32QAM	1.15*10-1	30.05	1544

Table 1: BER and SINR results from tank experiments

BER performance. To that end, we have performed experiments for different modulations, which are illustrated in Table 1. As it can be observed, we were able to reach data rates in the order of 1 megabit/s.

Sea Experiments. We have conducted further experiments at the Fish Harbor in Los Angeles, California. We have deployed 2 SEANet software prototypes connected to the acoustic front end discussed in Section 4 based on the Teledyne TC4038 approximately 10 m apart from each other at a depth of 4 m, with approximate total depth of 6.5 m. Similar to tank experiments, we used the ZP-OFDM scheme but this time over a frequency range of $500 - 800$ kHz.

Figure 6 illustrates experimental bit error rate (BER) results versus signal-to-noise ratio (SNR) for different modulation schemes with or without 3/4 convolutional coding. As it can be observed from the results, data rates of 522 kbit/s were achieved at sea over short horizontal links (i.e. 10 m) for a BER lower than 10^{-3}. Based on our previous experience, we anticipate that the BER will improve at least 2-3 orders of magnitude in open water as compared to the water tank and 1-2 orders of magnitude in open water as compared to harbor experiments for the same level of SNR.

Wireless Energy Transfer Experiments. We have conducted preliminary experiments by using the proposed energy transfer unit described in Section 4.1. We placed two TC4013 in a water tank 1 m apart from each other. We transmitted a 1 V_{p-p} sinusoidal signal at 125 kHz through a power amplifier with 30 dB gain. We measured a 0.2 V_{p-p} amplitude at the receiving end of the link right after the transducer. As a typical diode rectifier can work with $\sim$50% efficiency [37], we were able to obtain power in the order of mW.

6. CONCLUSIONS

We discussed the design of a new high-data rate software-defined underwater acoustic networking platform, SEANet G2, with unique characteristics in terms of data rates achievable, spectrum agility, and hardware/software flexibility in support of distributed networked monitoring operations. We described the hardware, software, and network architecture of the proposed platform. Moreover, we have demonstrated the potential for data rates in the order of megabit/s in a controlled lab environment and data rates of 522 kbit/s at sea over short horizontal link (i.e., 10 m) for a BER lower than 10^{-3}. We have also showcased the feasibility of acoustic wireless energy transfer.

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