Abstract—Due to continuous technology scaling, the nodal capacitances reduction and power supply voltage lowering result in an ever decreasing minimal charge capable of upsetting the logic state of memory circuits. CMOS circuits operating under sub-threshold voltage region are more susceptible than ever to externally induced radiation that is likely to bring about the occurrence of soft errors. Therefore, the robustness of the circuits against the soft errors is a requirement in nanoscale circuit designs. Since the previous soft error masking designs result in significant cost penalties in terms of power, area and performance when they applied to under $V_{th}$ operation, the development of low-cost hardened designs for storage cells is important. In this paper, a novel radiation hardened latch is presented for high performance sub-threshold voltage operation. The critical charge is increased five times than that of the conventional latch with only 10% of area increment including 46% of power reduction. This result caused by shortening delay and reduced power loss arose from it.

I. INTRODUCTION

Operating integrated circuits with a supply voltage below sub-threshold voltage is attractive since both static and dynamic power consumptions are strongly affected by the supply voltage [1], proportional to $CV_{DD}^2$ especially in CMOS digital circuits. Significantly reduced power is expected in the weak-inversion region operations when it is compared to the operations in strong-inversion region. However, there are many challenges to overcome including exponentially increasing delay with additional voltage scaling [2]. Most of all, soft error is a major concern in today’s deep sub-micron/nano technology, which is caused by $\alpha$-particles. When $\alpha$-particles from the packaging materials or neutrons from space penetrate a silicon wafer, they can generate a charge that perturbs the state nodes of memory element. This phenomenon is described as the occurrence of transient faults (TFs) [3]. If a TF is latched by a sampling element such as latch and flip-flops, it could result in a soft error (SE).

Soft error rate (SER), the ratio a certain device is expected to encounter soft errors, is dependent on technology scaling such as reduced nodal capacitances and lower voltages as well as shrinking dimensions to increases layout density [4]. Therefore, the susceptibility is becoming worse when the operation is under $V_{th}$ and radiation hardened latch design is becoming more important. Not only the increased SER, but also the performance of circuit is dramatically decreased due to the low supply voltage with channel length and supply voltage scaling. This is the motivation of this research, which focuses on design techniques to enhance the latch circuit’s performance with radiation hardened design at a similar or slightly increased area overhead.

Critical charge ($Q_{\text{crit}}$) is generally defined as the minimum amount of charge to change the state of the circuit following the strike of an ionizing particle at the sensitive node [5]. This is the nominal design factor of hardened latches and it is used as a reference for radiation hardening process. There have been many research articles on radiation gardened latch or flip-flop design. However, most of those works have either significant area overhead or increased power consumption issues. In this paper, a novel radiation hardened latch design is presented for high performance sub-threshold operation.

II. CONVENTIONAL HARDENED LATCHES

A. Reference Latch

Fig. 1. Conventional (unhardened) latch

Fig.1 shows a conventional latch circuit, which is not a hardened design. D denotes the input node, CLK and NCLK are the system clocks, INT1 is the internal feedback node, and Q is the output node of the latch. It has the feedback loop to retain the information during non-clock period. As reported in
[6], the different nodes have different TF’s susceptibility, and the critical charge($Q_{crit}$) is estimated only at specific nodes having the lowest $Q_{crit}$. Experimental result from simulation indicates that the lowest value of $Q_{crit}$ is the internal feedback node (INT1). Followings are several existing hardened latches that focus on increasing the critical charge of this node [7] or adding redundant feedback path to cover this weakness.

B. Existing Radiation Hardened Latches

There are few solutions to make circuits less susceptible to soft errors such as adding explicit capacitance [8], or adding redundant feedback path to mask soft errors. Most of the existing hardened latches use either of these. Fig.3 shows the hardened latches proposed in [7], which uses the bi-stable characteristic of Schmitt trigger and also increased the critical charge of internal feedback node. Schmitt trigger has a larger hysteresis property in voltage so that it can mask a transient pulse on the input [7]. Meanwhile, it also increases the critical charge of feedback node. However, a circuit using the Schmitt trigger cannot completely filter out transient faults affecting its feedback node and it shows quite debilitated performance under $V_{th}$ operation. Moreover, in case of Schmitt trigger latch proposed in [9], with only the basic structure of the Schmitt trigger circuit cannot drive logic high when the supply voltage is less than threshold voltage because of its bi-stable characteristic. Therefore, it is not possible to use in the sub-threshold voltage operation. Another latch (SIN-LC) with duplicating the internal node has been proposed in [3]. In this design, two inverters are added to the SIN-LC latch for a fair comparison with the reference latch design. However, the performance is worsened due to electrical conflicts between the transistors even though it can filter out the transient faults completely. The FERST latch proposed in [10] can reduce SER because of triple of the C-element. However, the area cost and power dissipation for hardening is too high, thus limiting its application in design.

III. PROPOSED LATCH

The proposed latch circuit schematic is shown in Fig.4. Here, like the circuit previously analyzed, D denotes the input node, CLK and NCLK are the system clock and negative clock respectively, Q is the latch output node, which should be invariant when CLK = 0, INT1 and INT2 are the feedback internal nodes of the circuit which, in the absence of external perturbations, assume equal logic value in both clock semi-periods, and INT3 and INT4 are internal nodes not belonging to the feedback loop. The basic radiation hardening concept is same as the one used in the latch proposed in [3]. However, the basic concept behind the proposed latch is to block the electrical conflict that takes place between the input driver and the conductive output transistors connected in series when CLK=1. This can be achieved by turning off the conductive output series transistors as soon as CLK switches for 0 to 1.

It is easy to verify under the fault-free case. When CLK=1, latch internal node INT1, the output of NAND gate, is logically 1 regardless of input D which leads to turn off the M2. In the same way, the internal feedback node of INT2, the output of NOR gate, is always logic 0 which turns off the transistor M3. Therefore, D propagates to the output Q without electrical disturbance and takes advantage of delay.
improvement. When CLK=0, the transmission gate (TG) is turned off and the two gates (NAND and NOR) are performed as inverters. Consequently, the previously charged output value is retained by the two feedback paths.

In case of transient fault affecting one of the internal feedback nodes INT1 or INT2, the output node Q does not flip because of the C-element part (inside of dashed area in circuit). If the two feedback node values are different because one node is affected by a transient fault, the output node becomes temporarily high impedance state without changing its logical value. On the C-element, flipping the output is only possible when both of the series transistors are affected by a transient fault. Triple structural C-element can be suggested to prevent the multiple nodes upsets. However, in consideration of the possibility and area consumption, it is less efficient. Similarly to the conventional latch in Fig 1, our proposed latch is transparent to TFs affecting the input node during the clock high phase. However, these TFs affecting the input during the clock enable time interval are not a significant concern since the output datum of the latch is not valid.

In this proposed design, we choose to use one transmission gate instead of the two TGs same in conventional latch since its operation can be an issue in sub-threshold voltage operation. Unlike the normal supply voltage operation, in the subthreshold voltage operation over V_th, TGs cannot drive logic high by itself. It is usual that peripheral circuit aids are required for the subthreshold operation. Therefore, as previously referred, certain circuits implementing with more than two TGs cannot operate properly. In the proposed latch, it results in the improvement of the latch performance by using less count of TGs.

IV. SIMULATION RESULTS

Several existing hardened latches are discussed in previous sections. Originally, these are not supposed to operate in sub-threshold voltage. However, the transistor aspect ratios are adjusted considering lower supply voltage operation and critical charge to compare the performance with the proposed radiation hardened latch. Extensive simulations have been performed to investigate the performance and the critical charge of these different hardened latches. All the simulations are performed with standard 0.18μm CMOS technology. Its absolute value of NMOS and PMOS threshold voltages are 480mV and 490mV, respectively. Also, considering the 3-σ variation margin [11], power supply voltage was chosen as 350mV. As the factor of SEs occurrence, the critical charges are selected from the lowest nodes values as mentioned in the previous section. In the reference latch, SEM, and ST latches, internal feedback node INT1 has the minimum Q_crit value while INT3 node has the minimum Q_crit value in the SIN-HR and the proposed latch. The data is measured using the same method used in [4], and the α-particle hitting phenomenon is modeled as double exponential current within non-clock period.

The simulation results show that the Q_crit value of the proposed latch is more robust than the value of the Schmitt trigger based latch, but less robust than the value of the SIN-HR latch. The results in Table I reveal that proposed latch’s Q_crit value is increased by 12% comparing with the ST-latch.

The performance of the different latches is compared based on the simulations of the switching characteristics of each latch for different values of data setup as proposed in [12], i.e. D_C-Q, D_D-Q in Fig 5. For these values, the maximum delay between positive and negative transitions (i.e. the larger value between high to low transition and low to high transition) is selected as the performance metric for latches. In the table I, the C-element based latches (SIN-HR and proposed) show shorter delay time than the Schmitt trigger based latch and the reference latch. This is because the later latches have two transmission gates while the former latches have only one transmission gate. Since the transmission gate cannot be completely turned on with the low voltage in subthreshold operation, the delay advantage of the single transmission gate is more manifest in low voltage operation. The proposed latch circuit has the NAND and NOR gates connected to CLK and Q as the inputs. This enhances the performance of input-output delay, which is related to the power dissipation as well. Unlike the operation under strong inversion region, the power dissipation results are highly relevant to the number of transmission gate. Therefore, the power dissipation of the proposed latch decreases 46%, 25%, and 8% for the reference latch, the ST-latch and the SIN-HR latch, respectively.

Fig. 6 shows the latch output nodes recovery from negative and positive glitches and the other nodes states when transition faults are occurred on the internal feedback node INT3 while the output of conventional latch shows flipped values.

<table>
<thead>
<tr>
<th>Latch</th>
<th>Reference</th>
<th>ST latch</th>
<th>SIN-HR</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q_crit(μC)</td>
<td>0.66</td>
<td>3.00</td>
<td>5.17</td>
<td>3.35</td>
</tr>
<tr>
<td>D_C-Q(μs)</td>
<td>3.73</td>
<td>3.02</td>
<td>2.43</td>
<td>2.39</td>
</tr>
<tr>
<td>D_D-Q(μs)</td>
<td>1.48</td>
<td>0.76</td>
<td>0.178</td>
<td>0.136</td>
</tr>
<tr>
<td>Power(pW)</td>
<td>137</td>
<td>98.94</td>
<td>80.71</td>
<td>73.84</td>
</tr>
</tbody>
</table>

Table I

Performance Comparison of Latches

![Fig. 5. Timing diagram](image-url)
The effect of process variations on soft error tolerance is increased with technology scaling [7]. The soft error tolerance of the latches is also evaluated in the process variations. In this paper, Monte Carlo simulation based on 1K samples is used to assess the latch design under PVT variations. Parameters including voltage and various processes (threshold voltage, channel length, gate oxide thickness and so forth) are swept and simulations are run using a ±5% Gaussian distribution with Monte Carlo simulation PVT variation model. Table II shows the failure probability of the reference latch, the ST latch, the SIN-HR, and the proposed latch when a fixed charge of 3.35fC is applied to the critical node of each latch. 3.35fC is the critical charge of the proposed latch. The result of Table II confirms that if the induced charge is constant, then the probability of failure of hardening is smaller when a larger $Q_{crit}$ is present in the latch. Also, it reveals that the process variation affects significant impact on soft error tolerance by looking at the failure probability of the SIN-HR latch.

<table>
<thead>
<tr>
<th>Latch</th>
<th>Critical Charge (fC)</th>
<th>Hardening Failure Prob @ 3.35fC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference</td>
<td>0.66</td>
<td>100%</td>
</tr>
<tr>
<td>ST latch</td>
<td>3.00</td>
<td>100%</td>
</tr>
<tr>
<td>SIN-HR</td>
<td>5.17</td>
<td>16.55%</td>
</tr>
<tr>
<td>Proposed</td>
<td>3.35</td>
<td>60.90%</td>
</tr>
</tbody>
</table>

V. CONCLUSION

This paper presented a new novel design for the radiation hardened latch circuit operating at sub-threshold voltage in nano scale CMOS. Simulations demonstrate that the proposed design has excellent tolerance to soft errors with low input-output delay, low power consumption, and high performance in subthreshold operation. These figures of merit have been comprehensively assessed and verified. The proposed latch has the shortest delay and lowest power dissipation among the compared latches. Even though area is slightly increased, for the reason of short input-output delay, the proposed latch consumes less power than existing low performance latches.

REFERENCES