A Built-In Calibration System with A Reduced FFT Engine for Linearity Optimization of Low Power LNA

Yongsuk Choi, Chun-hsiang Chang, In-Seok Jung, Marvin Onabajo, Yong-Bin Kim
Dept. of Electrical and Computer Engineering
Northeastern University, Boston, USA
ychoi@ece.neu.edu, cchang@ece.neu.edu, jung.i@husky.neu.edu, monabajo@ece.neu.edu, ybk@ece.neu.edu

Abstract—A digital built-in calibration (BIC) system with a power and area optimized on-chip fast Fourier transform (FFT) engine is presented to automatically adjust the linearity of a tunable RF low-noise amplifier (LNA) operating at 2.4GHz. An envelope detection circuit is used to extract the linearity characteristics at low frequencies, enabling the sampling and digital signal processing at low rates. To compensate the low gain of an envelope detector and to enhance reliability of spectral analysis, an RF amplifier is designed between the LNA and the envelope detector. The output of the envelope detector is digitized before the spectrum calculation with the integrated FFT for estimation of the third-order intermodulation (IM3) distortion specification of the LNA. The digitally-assisted closed-loop calibration scheme is demonstrated with simulations using a two-tone test with 1MHz tone spacing, a 512-point FFT engine, a 10-bit analog-to-digital converter model, and digital blocks operating with a 51.2MHz clock frequency. The total time required for calibration is 485µs including delays of 1.2µs to allow settling of the LNA output after capacitor array changes for tuning. In order to validate the proposed BIC technique with device mismatch effects, Monte Carlo simulations are performed with the same condition at transient simulations, where the results are well matched with the optimum IM3 component values calculated at the output node of LNA. The digital blocks were implemented using a standard 0.13µm CMOS technology.

Keywords – Low-noise amplifier (LNA), third-order intermodulation, linearization, analog/RF testing, envelope detection, fast Fourier transform (FFT), spectral analysis, built-in calibration (BIC)

I. INTRODUCTION

Improvement of the integrated CMOS technology allows systems-on-chip (SoC) designs that include mixed signal circuits are widely used. At the same time, their applications in communications, signal processing, and embedded systems are also increasing. As higher specifications are required for analog circuits due to new applications, the performance of the circuits has kept improving. In the meantime, the increase of CMOS technology devices scaling and its variability require more testing/tuning after fabrication. It is critical to enhance the quality and yield of integrated circuits in CMOS technologies, especially in analog/RF circuits that are more vulnerable to process variations and aging effects. Therefore, design for optimum performance alone is insufficient to prevent performance degradations from those effects. Built-in calibration (BIC) is an attractive and practical approach that allows to improve testing and parameter tuning capability as well as to improve reliability and lifetime of a circuit under test (CUT). Not only reduction of testing costs and time by decreasing the reliance on off-chip test instruments and the number of I/O pin counts, but also extension of the circuit lifetime by periodic on-chip measurement and calibration are main benefits of the BIC technique superior to the conventional off-chip measurement.

In Fig. 1, a diagram of a wireless receiver with adjustable analog front-end blocks is shown. It is illustrated that linearity and gain tuning for low-noise amplifiers (LNAs), second-order nonlinearity and mismatch correction for mixers, linearity enhancements and frequency tuning for bandpass filters, and gain tuning for variable gain amplifiers (VGAs) are enabled by collaborating with digital resources such as digital signal processors (DSPs). [1]-[4] are some examples showing the analog designs with digitally-assisted tuning capabilities. An important aspect of measuring parameters such as gain and linearity is the ability to evaluate the performance of a CUT at various frequencies based on spectral characteristics. Conventionally, high-performance equipments such as a spectrum analyzer and a logic analyzer are used to get the spectral analysis, which is necessary in the BIC technique as well. As a result, there is an increasing need for efficient on-chip digital resources for on-chip spectral characterization and digital calibration control to provide the essential feedback loop for understanding the characteristics of the manufactured devices. Toward this goal, there are some approaches involving in the correlation of a circuit's envelope response. In [5], for example, an envelope detector, ADC, and digital signal processor are utilized for self-calibration. Moreover, it was proposed in [6] to evaluate the output spectrum of an envelope detector connected to the output of a CUT for extraction of third-order distortion, which requires the implementation of an on-chip FFT engine.

One of the main challenges in designing the BIC systems is...
to build a low cost calibration circuitry while maintaining sufficient accuracy. Fig. 2 shows the block diagram of a digitally-controlled BIC system to estimate a device non-linearity factor of an RF CUT, the third-order intermodulation (IM3) of a LNA, and to automatically tune for optimum IM3 performance designed in [7]. A FFT engine design approach from [8] as well as a magnitude estimator for complex numbers are employed for area-efficient spectral analysis hardware design. Furthermore, the spectral analysis at low frequencies are desired to decrease qualification of an analog-to-digital converter (ADC) and operational speed of digital circuits. In Fig. 2, the envelope detector is a down-converter which has spectral information of LNA outputs. It also makes it possible for ADC and digital blocks to operate in low frequency range.

In this research, two design techniques are applied in the BIC system to develop an estimation of the IM3 of RF CUT and to automatically tune for optimum IM3 performance. Instead of conventional FFT architectures, a reduced and optimized FFT engine is proposed for the purpose of built-in calibration. In addition, an RF amplifier is employed between the RF CUT and an envelope detector to compromise the low gain of the envelope detector used as a down-converter. The LNA topology from [9] is used as a reference circuit to demonstrate the functionality of the BIC system. It contains digital switches that allow tuning of the IM3.

The remainder of the paper is organized as follows. In Section II, a digital built-in calibration architecture, a tunable LNA circuit, and subsequent analog circuits such as an RF amplifier and an envelope detector are discussed with simulated performance information. The IM3 component estimation principle and sampling frequency determination technique are introduced in Section III. In Section IV, summarized digital hardware implementation and a proposed power and area optimized computational FFT engine for BIC application are presented. The simulation results of the calibration system including the proposed FFT engine are then shown in Section V, followed by the conclusion in Section VI.

II. CALIBRATION SYSTEM COMPONENTS AND CUT

A. Calibration Architecture

In Fig. 2, a block diagram of a calibration method in [7] is displayed. To estimate the non-linearity of the LNA, IM3 components and a two-tone input signal is applied, and frequencies of the LNA output signal are down-converted through an envelope detector. The down-conversion avoids the use of an ADC with a high sampling frequency, which would be challenging to design and would consume excessive power. After the envelope output signal is digitized by the ADC, it is analyzed in frequency domain using an FFT engine with a clock frequency equal to the ADC sampling frequency. An IM3 calculator in the digital calibration unit estimates the IM3 magnitudes from the FFT outputs that are complex numbers. Once the first cycle of the IM3 estimation process is completed, the controller block changes the switch combination of the capacitor array to adjust the IM3 of the LNA before repeating the IM3 evaluation process. During every cycle, the output of the IM3 calculator is compared with the previous output, and the smaller value (indicating better IM3 performance) is stored in a register as a best case. This process is iterated with different combinations of an N-bit capacitor array within the LNA. The controller block controls the other digital blocks and applies the best combination of the capacitor array when the tuning procedure is completed. Details of the IM3 component extraction from the output of the envelope detector are discussed in sections III.

B. Tunable Low-Noise Amplifier for Low Power Application

In Fig. 3, the schematic of the cascode LNA with inductive source degeneration is shown from our previous work, in which this subthreshold LNA with linearity enhancement was proposed [9]. TABLE 1 lists the main specification parameters of the linearized LNA design in [9] from simulations with several Cgd2_ext values, where Cgd2_ext can be implemented with a fixed capacitor (Cgd2_ext = 90fF) and a 3-bit digitally-programmable capacitor (Cgd2_ext = 20fF, Cgd2_ext = 40fF, and Cgd2_ext = 80fF) as depicted in Fig. 3. The maximum and minimum capacitance values occur with S2,3,2,1 = [000] and S2,3,2,1 = [111] respectively, where ‘0’ or ‘1’ indicate that the switch is connected to ground or the supply voltage, respectively. The results in TABLE 1 reveal that changes of Cgd2_ext have minor
effects on \( S_{11}, S_{21} \) and noise figure. The IM3 values in TABLE 1 are from two-tone test simulations with -25dBm input power, and the best IM3 occurs at \( S_{32,1} \). Hence, the proper \( L_{g2} \) and \( C_{g'd2,ext} \) values have been selected for optimum third-order distortion cancellation in the presented example design. Furthermore, the IM3 performance can be optimized after fabrication by tuning \( C_{g'd2,ext} \).

C. Envelope Detector and Cascode RF Amplifier

For on-chip testing and calibration, a low cost and accurate high frequency signal analysis should be realized. Fig. 4 shows the envelope detector used as down-converter [10]. The envelope detector was designed using vertical bipolar (PNP) transistors in a standard 0.13µm CMOS technology. The BJT has better linearity and higher dynamic range than NMOS or diode. Therefore, the BJT is adequate for BIC with the simple circuitry. (Even though the vertical NPN devices have a low current gain (\( \beta = 8 \)) and limited linearity characteristics, the simulation results in Section V confirm that the envelope detector performance is adequate to process 2.4GHz input signals. ) However, the CUT is low power application and the input power level is around -30dBm. Also, on account of a low current gain (\( \beta = 8 \)) from vertical NPN devices and limited linearity characteristics, additional amplifier is required before the envelope detector stage. Fig. 5 is a cascode common source RF amplifier with 12.8dB gain which provides more reliable results by compensating the envelope detector for low gain in analyzing spectral components. Even though the envelope detector and the RF amplifier also create nonlinearities, the estimation performance is not significantly affected, because the calibration is conducted with the same envelope detector and RF amplifier nonlinearity conditions as the LNA settings are changed to determine the optimum output IM3.

III. CALIBRATION PRINCIPLES

A. IM3 Components Estimation

Fig. 6 visualizes a two-tone test for the characterization of an RF circuit (CUT) with an envelope detector to down-convert high-frequency signals to low frequencies. The signal \( x(t) \) is a test input with two tones having an amplitude of \( A \), where the tones have a frequency spacing of \( \omega_h \). The output signal \( y(t) \) is denoted with fundamental magnitudes of \( B_1 \) and third-order nonlinear components (\( B_2 \)) created by the CUT. The signal \( r(t) \) is the envelope response of \( y(t) \), which can be expressed as [6]

\[
r(t) = 2 \cdot B_1 \cdot \sin\left(\frac{\omega_h t}{2}\right) + 2 \cdot B_2 \cdot \sin\left(\frac{3\omega_h t}{2}\right),
\]

(1)

\[
b_k = \frac{8}{\pi} \left( \frac{B_1(-1)^{k+1} + 3B_2(-1)^k}{4k^2 - 1} \right)
\]

(2)

Equation (2) shows that every harmonic component in the spectrum of \( r(t) \) can be expressed as a linear combination of the magnitude of \( B_1 \) and \( B_2 \). The magnitude of \( B_2 \) represents the third-order intermodulation product. Therefore, the IM3 component can be extracted from two of the measured \( b_k \) values. Since \( b_0 \) is the DC component and high-order harmonic components are too small to be measured accurately, the \( b_1 \) and the \( b_3 \) components are chosen in this work to estimate the magnitude of \( B_2 \). Two equations can be obtained from (2) and written in matrix form:

\[
\begin{pmatrix} b_1 \\ b_3 \end{pmatrix} = M \begin{pmatrix} B_1 \\ B_2 \end{pmatrix}, \quad M^{-1} = \begin{pmatrix} 0.9378 & 2.8114 \\ 0.2410 & -2.8114 \end{pmatrix}
\]

(3)

\[
x(t) \xrightarrow{\text{CUT}} y(t) \xrightarrow{\text{Envelope Detector}} r(t)
\]

Fig. 6. Two-tone test with an envelope detector.
The inverse matrix of $M$ in (3) presents the coefficients for the linear combination of $B_1$ and $B_2$ to reproduce the magnitude of $B_2$ from a down-converted signal $r(t)$.

B. Sampling Frequency Determination

To accurately estimate IM3 components and to minimize the digital hardware complexity, especially of the FFT engine, the coherent sampling method from [8] is used. The fundamental frequency of the ADC input signal is same as the spacing of the test tones. The sampling frequency of the ADC, FFT engine and the clock frequency of the digital blocks are

$$f_s = \frac{\Delta f \cdot N_{FFT}}{M_{cycle}}, \quad (4)$$

where $f_s$ represents a sampling frequency, $N_{FFT}$ is the size of the FFT engine, $M_{cycle}$ is an integer number (prime number in general) of cycles in the sampled set, and $\Delta f$ is the test tone spacing. From (4), the sampling frequency would be 51.2MHz with a 512-point FFT engine, 5 cycle for sampling and 500kHz tone spacing.

IV. DIGITAL HARDWARE IMPLEMENTATION

The digital hardware including FFT engine, IM3 calculator, controller and registers are designed with the Verilog hardware description language (Verilog-HDL), and synthesized with a standard 0.13µm CMOS process technology. The layout of the digital calculation unit (FFT engine is not included here) is shown in Fig. 7, which occupies 190×190µm² of silicon area. A proposed FFT engine is different from conventional FFT and optimized for BIC application to process only few interested spectral results.

A. Proposed FFT Engine for BIC Applications

The discrete Fourier transform (DFT) $X_k$ of a $N$-point discrete-time signal $x_n$ is defined by:

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}, \quad 0 \leq k \leq N - 1, \quad (5)$$

where $W_N$, the twiddle factor, is defined as

$$W_N = e^{-j2\pi/N}, \quad k = 0 \text{ to } N - 1. \quad (6)$$

However, a straightforward implementation of this algorithm is inefficient due to the huge hardware specification and latency. The FFT is a class of efficient DFT implementations that produce results identical to the DFT while it speeds up computation time and reduces the hardware cost. Generally, decimation-in-time (DIT) and decimation-in-frequency (DIF) are two most widely recognized Cooley-Tukey algorithms. In this work, the DIF decomposition is adopted because it matches the manipulation manner of partial processing element (PE) selection. Also, single delay feedback (SDF) facility has an advantage in hardware overhead trading off for low throughput.

From the sampling method in [8] and (4), not all the components of FFT outputs are needed for BIC spectral analysis. Given that area overhead is one of the challenges in on-chip calibration techniques, designing an optimized FFT engine with only essential parts provides a benefit in terms of area and power consumption as well. Moreover, different from the conventional FFT, only real-valued data are sampled in time domain because imaginary part is not required in this application. That is, complex number multipliers and adders can be eliminated at the first PE stage. An example of radix-2 DIF FFT signal flow graph (SFG) for $N=16$ is shown in Fig. 8. If $X[0]$ and $X[8]$ are the only values required to extract information from CUT, the top butterfly (dotted line) stages in each PE are requirement for analysis and calibration. By removing the unnecessary information and hardware, the FFT engine can optimize the number of adders and multipliers while shortening the latency of processing.

A 512-point FFT engine is desired for reliable spectral outcomes with a combination of a 10-bit ADC. Most of the intermediate stages and output values are redundant and can be optimized in this method. From (4), the two components for spectral analysis are the second and fourth discrete frequencies (often named bins), which correspond to 500kHz and 1.5MHz frequency bins, respectively. Therefore, the proposed FFT engine carries out operation only for the two bins. This frequency bins are selected from two-tone test setup, however, the test condition can be changed with different input frequencies. Also, using the same PE, the FFT engine can have flexible outputs with reconfigurable design. Therefore, the low throughput is less important than in conventional FFT engine because of the limited FFT outputs in the proposed engine.
A single Radix-4 DIF butterfly is designed in each stage for each bin calculation. Even if there are four parallel pipelined PE, a single PE is designed and others are abandoned. Equation (5), the N-point DFT, can be decomposed as N/4-point FFTs, or

\[ X(4k) = \sum_{n=0}^{N/4-1} x(n) + x(n + N/4) + x(n + N/2) + x(n + 3N/4) ]jW^kN \]

\[ X(4k + 1) = \sum_{n=0}^{N/4-1} x(n) - js(n + N/4) - x(n + N/2) + js(n + 3N/4) ]jW^kN \]

\[ X(4k + 2) = \sum_{n=0}^{N/4-1} x(n) - x(n + N/4) + x(n + N/2) - x(n + 3N/4) ]jW^2kN \]

\[ X(4k + 3) = \sum_{n=0}^{N/4-1} x(n) + js(n + N/4) - x(n + N/2) - js(n + 3N/4) ]jW^3kN \] (7)

for \( k = 0 \) to \( N/4-1 \), where \( W^c = W_{N/4}^c \).

In comparison with the conventional FFT designed in the previous work in the same technology, the area and power consumption is decreased from 4.31mm\(^2\) and 68.3mW to 0.51mm\(^2\) and 5.0mW, respectively at 51.2MHz of clock speed. Also, the proposed FFT is designed as 5 cycles of latency after sampling 512 data points.

V. SIMULATION RESULTS

In this section, results are reported to demonstrate the linearity calibration technique for the example LNA using the analog/mixed-mode simulation (AMS) environment in Cadence to assess the analog circuits and digital blocks (implemented with Verilog-HDL). Here, \( C_{gd2,ext} \) is varied from 90fF to 230fF with a 20fF step size. The two LNA input tones (with -30dBm of input power levels) are located at 2.4GHz and 2.4005GHz. The 500kHz tone spacing results in low-frequency envelope detector output components with 500kHz spacing. The sampling frequency of the ADC and the digital clock frequency based on (4) is 51.2MHz. The full scale input range of the 10-bit ADC is from 0.4V to 1.2V. The digital clock frequency based on (4) is 51.2MHz. The full scale input range of the 10-bit ADC is from 0.4V to 1.2V. The ADC is a behavioral block in the simulation. However, the ADCs in [11] would meet the design specification. TABLE 2 contains a summary of a closed-loop transient simulation result. The best code is [100] and IM3 component value is 33.15dBc, which is the optimum value among all the cases. This optimum setting can be identified from the minimum “estimated IM3” number in TABLE 2. It represents the magnitude of the third-order intermodulation component extracted by the IM3 calculator. The total simulation time is 485\( \mu \)s including delay of 1.2\( \mu \)s to allow settling of the LNA output after capacitor array changes. Fig. 9 visualizes IM3 component values before the closed-loop calibration with device mismatch statistic. From 200 samples, the actual IM3 component values are distributed from 30.71dBc to 31.87dBc before the performance optimization. Monte Carlo simulation results after tuning algorithm with the same device mismatch statistic are shown in Fig. 10. The best code from calibration results are matched with the optimum IM3 component values calculated at the output node of LNA in all cases. The actual optimum IM3 component values are spread out from 32.41dBc to 33.85dBc. In the closed-loop transient simulation, RF device model is used as NMOS which has additional model parameters to characterize at high frequency operation. In the meantime, process variations are considered in the mismatch model parameters, but some of the RF characteristic factors are not included in it. Consequently, there are minor different results between the two conditions, and the optimum IM3 value (35.57dBc) in the TABLE 1 is not in the range of IM3 component values after calibration as shown in Fig. 10.

![Fig.9. Initial IM3 component values before tuning with device mismatch.](image)

![Fig.10. Monte Carlo simulation results after calibration and tuning with device mismatch.](image)
VI. CONCLUSION

A built-in calibration system for performance tuning of RF amplifiers with optimized FFT engine was presented. This architecture allows on-chip calibration for linearity optimization by estimating the IM3 during two-tone testing. To minimize the area and power overhead of the system, an envelope detector was employed to reduce the speed of operation for the ADC and digital blocks, and an efficient IM3 estimation method has been developed. Closed-loop simulations of this calibration system and a low-noise amplifier with digitally-tunable third-order linearity performance showed the feasibility of the synthesized digital blocks in standard CMOS technology with device mismatch statistic. In conclusion, the proposed calibration system for RF amplifier linearity tuning enables performance-enhanced designs with higher tolerance against process variations, reduced manufacturing test costs, and product lifetime extension through periodic calibrations. This paper will be a good reference for future built-in self calibration circuits for analog and mixed-mode circuits.

REFERENCES


226 2014 International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)