Calibration Technique Tracking Temperature for Current-Steering Digital-to-Analog Converters

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Abstract—In this paper, a novel foreground calibration technique is presented for current-steering DACs. Each current source is in parallel with a CAL DAC injecting a small correction current that corrects the mismatch and tracks the temperature variations. High matching accuracy is not only achieved at the calibration temperature, but also maintained across a wide temperature range from $-40^\circ C$ to $120^\circ C$. A 14-bit DAC is designed in a standard 65nm CMOS process to verify the concept. The transistor level simulation results show that the new calibration technique reduces the worst case INL and DNL of the DAC across the whole temperature range by a factor of 15.7 and 12.8 compared with the intrinsic matching and by a factor of 2.9 and 2.8 compared with the conventional calibration method [1]. The DAC achieves real 14-bit level INL and DNL across a wide temperature range with only 10-bit level raw matching.

I. INTRODUCTION

Current-steering digital-to-analog converters (DACs) are widely used to generate analog signals across a wide speed and resolution range. In many high accuracy applications, it is important that the current sources of a DAC are highly matched. The mismatches between the current sources directly affect the DAC's static linearity.

The random device mismatch causes the current mismatch of the current sources, which drifts with the varying operational temperature. This effect exacerbates the mismatch problem.

A straightforward method to reduce the device mismatch is to increase the device physical area. This becomes unrealistic for more than 12 bit accuracy because the area grows by a factor of 4 for 1 bit accuracy improvement. On the other hand, the calibration techniques improve the current mismatch without increasing the device area. There have been extensive researches on the calibration techniques, but limited research on their temperature-tracking capability.

[2]–[4] implemented background calibration techniques to continuously calibrate the current sources during normal operation. These techniques may track the operating condition changes, but they consume extra power due to the continuous operation and may degrade the DAC’s performance due to extra noise and spurs.

The foreground calibration techniques [1], [5], [6] alleviate these disadvantages. An auxiliary DAC, named CAL DAC, provides the correction current to the current source to be calibrated. The mismatch information is stored in digital format in RAM or non-volatile memory as the input of the CAL DAC. Therefore, these techniques consume less power and do not introduce noise or spurs during normal operation. However, the existing foreground calibration techniques do not track temperature, as mentioned in [1]. Recalibration is usually required when the temperature varies.

In this paper, a foreground calibration technique capable of tracking across temperature is presented. The temperature dependence of the current mismatch is identified. Similar to [1], CAL DACs are implemented to provide the correction current for each current source, but the correction current tracks the current source mismatch change with temperature. Therefore high accuracy over a wide temperature is achieved.

This paper is organized as follows. Section II discusses the mismatch of current sources and its temperature dependence. Section III presents the new calibration technique and its implementation in a 14 bit DAC. Section IV presents the transistor level simulation results, followed by the conclusions in Section V.

II. CURRENT MISMATCH

The current sources of a DAC are usually designed with long channel devices and biased in saturation region. The square law

$$I = \frac{\mu C_{ox} W}{2} (V_{GS} - V_{TH})^2 = \frac{\beta}{2} (V_{GS} - V_{TH})^2 \quad (1)$$

is accurate enough to characterize the I/V relation of a transistor even in the advanced fine-line process.

The mismatch of the two closely spaced, identical MOS transistors can be quantified using Pelgrom’s model [7]. The threshold voltage differences $\Delta V_{TH}$ and relative current factor differences $\Delta \beta/\beta$ are two major mismatch parameters. The random difference of many matched pairs obeys a normal distribution with zero mean and a variance dependent on the device area.

Two current sources consisting of identical PMOS transistors with the same $V_{GS}$ are shown in Fig. 1. The current mismatch between $I_1$ and $I_2$ is given by

$$\Delta I = \frac{\Delta \beta}{\beta} I - g_m \Delta V_{TH} \quad (2)$$

where $I$ is the nominal current and $g_m = \sqrt{2\mu C_{ox}(W/L)}I$ is the nominal transconductance. $I$ is usually designed to be temperature independent. $g_m$ is a function of both the bias.
current $I$ and temperature since the mobility $\mu$ is temperature dependent. Fig. 2 shows the simulation result of $g_m$ of a typical long channel PMOS with the constant current 2.5 mA. $g_m$ shows a strong dependence on the temperature, as it varies 50% as the temperature changes from $-40^\circ C$ to 120 $^\circ C$.

In a typically biased current source, $|g_m \Delta V_{TH}|$ is usually much larger than $|((\Delta \beta/\beta))I|$ and dominates the total current mismatch. Therefore,

$$\Delta I \approx -g_m \Delta V_{TH}$$

(3)

The temperature dependence of $\Delta V_{TH}$ is measured in [8]. The conclusion is that “the standard deviation of threshold-voltage mismatch is practically constant” with respect to temperature. $\Delta V_{TH}$ is considered as constant in this work. Therefore, the temperature dependence of $g_m$ determines the temperature dependence of the current mismatch.

III. NEW CALIBRATION TECHNIQUE

Based on the previous discussion, it is easy to understand why the calibration technique in [1] does not track the temperature. The configuration of the current source with CAL DAC in [1] is shown in Fig. 3. $M_{cal}$ provides the reference current of the CAL DAC $\alpha I$ which is proportional to $I$ because $M_{CS}$ and $M_{cal}$ share the same gate voltage. $\alpha$ is much less than 1, 1/32 in [1], because $M_{cal}$ only needs to provide the mismatch current of $M_{CS}$. The transistors from $M_{s0}$ to $M_{sn}$ forms a 6-bit current splitter. The switches from $S_1$ to $S_n$ are controlled by the digital inputs to steer the branches of the current splitter to either the drain of $M_{CS}$ or ground. After the current source $M_{CS}$ is calibrated at a certain temperature $T_{cal}$, the CAL DAC current is equal to the current mismatch at $T_{cal}$. The CAL DAC digital value is $(g_m(T_{cal})\Delta V_{TH})/(\alpha I)$. When the temperature varies, the current mismatch of $M_{CS}$ will change due to $g_m$, whereas the CAL DAC output still keeps the snapshot of the current mismatch at $T_{cal}$, i.e. $g_m(T_{cal})\Delta V_{TH}$. The CAL DAC does not track the current mismatch. The linearity of the DAC degrades with the varying temperature.

A. New DAC Calibration Technique

The new calibration technique still includes a CAL DAC in parallel with each current source as shown in Fig. 4. The difference is that the reference current of the CAL DAC is proportional to $g_m V_c$, where $V_c$ is a constant voltage derived from the bandgap voltage. When the current source is calibrated at $T_{cal}$, $(g_m(T_{cal})\Delta V_{TH})/(g_m(T_{cal})V_c)$, i.e. $(\Delta V_{TH}/V_c)$, is captured and stored as the CAL DAC digital value. When the temperature varies to $T$, the CAL DAC output current is equal to $g_m(T)\Delta V_{TH}$, which still track the current mismatch at the new temperature. Identifying the temperature dependence of the current mismatch and using the replica to track it are the keys of the new technique.

B. DAC Configuration

A 14-bit DAC is designed to verify the proposed calibration technique. The DAC segmentation is 4-4-6, i.e. 4 most significant bits (MSBs), 4 intermediate significant bits (ISBs) and 6 least significant bits (LSBs). The DAC current sources are implemented using PMOS transistors. The MSB segment is thermometer coded and consists of 15 MSB current sources $M_{CS,MSB}$. There are 16 ISB current sources $M_{CS,ISB}$. 15 of them belong to the thermometer coded ISB segment. The 16th $M_{CS,ISB}$ is subdivided to provide the remaining 6 binary
coded LSBs using a current splitter. The width of $M_{CS,MSB}$ is 16 times as large as the width of $M_{CS,ISB}$. The DAC reference current is 40 mA. Each $M_{CS,MSB}$ is 2.5 mA and each $M_{CS,ISB}$ is 156.25 $\mu$A. The 14-bit level LSB is 2.44 $\mu$A.

The calibration configuration is shown in Fig. 5. Each current source is connected with a new CAL DAC. Each CAL DAC is 6 bits and the resolution is about 1/8 14-bit level DAC LSB. Based on the foundry measurement results, the standard deviation of the random mismatch of $M_{CS,MSB}$ is 1.94 $\mu$A. The reference current of the CAL DAC is 19.52 $\mu$A and large enough to cover the 6$\sigma$ range. The cascode switches $M_{CAS1}$ and $M_{CAS2}$ steer the current to the calibration circuitry during its calibration or to the DAC outputs during normal operation. The current splitter of the LSB segment relies on its intrinsic mismatch. All 16 $M_{CS,ISB}$ current sources including the sum of the LSB segment are measured against $I_{ref}$ first. Then 15 $M_{CS,MSB}$ current sources are measured against the sum of all ISB and LSB segments to eliminate the boundary from ISB to MSB. During each measurement, the difference is adjusted to approach zero through the successive approximation register (SAR) logic.

**C. $g_mV_c$ Current Generator**

A $g_mV_c$ current generator, shown in Fig. 6, is needed for the CAL DACs. There is a sub circuit called “$I_R$ generator” inside “$g_mV_c$ current generator”. The voltage across $R_I$ is forced to the bandgap voltage, $V_{BG}$, by the amplifier $A1$. The current, $I_{RI}$, is equal to $V_{BG}/R_I$ and fed into the two resistors, $R_1$ and $R_2$, with the same value $R$. $R_1$ and $R_2$ are the same type of on-chip resistors. The voltage across $R_1$ and $R_2$ is $(V_{BG}R)/(R)$, which is a constant fraction of the bandgap voltage. $V_{GS}$ is the gate voltage of the current sources generated by the DAC bias circuit. $M1$ and $M2$ are replicas of $M_{CS,MSB}$ with the same $g_m$. Therefore the gate voltages of the differential pair $M1$ and $M2$ are $V_{GS} + I_R R_1$ and $V_{GS} - I_R R_1$, respectively.

The output current, $I_{gm}$, is equal to the current difference of $M1$ and $M2$,

$$I_{gm} = \frac{\beta}{2}(V_{GS} + I_R R - V_{TH})^2 - \frac{\beta}{2}(V_{GS} - I_R R - V_{TH})^2$$

(4)

$$= g_m \times 2I_R R.$$  

(5)

By defining $V_c$ to be $2I_R R = (2V_{BG} R)/(R_I)$ as a constant voltage, the output current $I_{gm}$ becomes $g_m V_c$.

**IV. TRANSISTOR LEVEL SIMULATIONS**

The DAC is implemented in a 65 nm CMOS process. The simulations are performed with BSIM4 models. Random mismatches are attached to each transistor with the mismatch parameters provided by the foundry. $\Delta/\beta$ is equally divided into the mismatch of width, length and gate oxide thickness. $\Delta V_{TH}$ is modeled in the parameter $V_{TH0}$. Both $\Delta/\beta$ and $\Delta V_{TH}$ are constant in the simulations.

Three scenarios are simulated for illustration. In the first scenario, there is no calibration and the DAC purely relies on the intrinsic matching of the current sources. In the second and third scenarios, the DAC is calibrated at 40$^\circ$C using the technique in [1] and the proposed technique, respectively. After the calibration is done, the temperature is swept and the temperature drift of the DAC performances are obtained.

**A. Current Sources Temperature Drift**

The currents of 15 $M_{CS,MSB}$ versus the temperature of three simulation scenarios and the distributions of the temperature drift are shown in Fig. 7. The temperature drift in the histograms is defined as the difference between $-40^\circ$C and $120^\circ$C for a current source. The calibration technique in [1] forces the 15 $M_{CS,MSB}$ within the resolution of the CAL DAC under the calibration temperature 40$^\circ$C. The currents diverge when the temperature drifts high or low. The new calibration technique reduces the distribution sigma to 0.22 LSBs across the whole temperature range.

The calibration technique in [1] does not improve the drift compared to the scenario without any calibration because the CAL DAC output current is temperature independent. The new technique improves the standard deviation of the temperature drift by a factor of 2.3. The remaining drift is caused by the ignored $(\Delta/\beta) I$ component of the current mismatch.
INL AND ◦ DNL (− ◦ 150 to ◦ 100 to ◦ 0) as shown in Fig. 2. With the current M ◦ 100 − 5 ◦ 0 to 0 ◦ 50 150 ◦ 100 ◦ 50 100 ◦ 0 ◦ DNL (14-bit level LSB) 6.02 0.46 0.16 3.33 μ 0.32 7.21 < 0.92 IEEE J. Solid-State Circuits and −, “The temperature dependence of at CAL T dbm/Hz noise power spectral
1.35 W
Worst case
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ing temperature is presented. The temperature dependence
of 8.6 compared with the technique in [1].
are factors 246 compared with no calibration and by a factor
intrinsic matching and by a factor of 2.9 and 2.8 compared with the conventional calibration method [1].
From the area perspective, 1-bit linearity improvement requires quadruple the device area. Therefore, for the same INL, this technique reduces the area of the current sources by a factor of 246 compared with no calibration and by a factor of 8.6 compared with the technique in [1].
V. CONCLUSION
In this paper, a new foreground calibration technique tracking temperature is presented. The temperature dependence of the current source mismatch is identified and CAL DAC tracking temperature is introduced. A transistor level 14-bit DAC is implemented in a standard 65nm CMOS processes to verify this technique. Simulation results show a significant linearity improvement across a wide temperature range from −40 ◦ C and 120 ◦ C, compared with the intrinsic matching and the conventional calibration method [1].

REFERENCES