A 90 nm High Volume Manufacturing Logic Technology Featuring Novel 45 nm Gate Length Strained Silicon CMOS Transistors


Logic Technology Development, * TCAD, # QRE

Intel Corporation, Hillsboro, OR, USA
90 nm Logic Technology Features

- Strained Silicon Transistors
- 1.2 nm Gate Oxide
- Nickel Salicide
- 7 Copper Interconnect Layers
- Low-k CDO Dielectric
- 1.0 $\mu$m$^2$ SRAM Cell

S. Thompson, et. al., 2002 IEDM
Transistor Strain Techniques

Traditional Approach

- Graded SiGe Layer
- Biaxial Tensile Strain

This Technology

- Selective SiGe S-D
- Uniaxial Compressive Strain

- Tensile Si₃N₄ Cap
- Uniaxial Tensile Strain
Strained PMOS Structure

- SiGe film embedded into source/drain
- SiGe film deposited by selective epitaxy
- Induces large uniaxial compressive strain in channel
- Dramatic hole mobility enhancement

Embedded Geometry + Compressive S/D = Large Uniaxial Channel Strain
Strained PMOS Process Flow

- SiGe introduced late in the process flow → source-drain
- Si Recess Etch + SiGe Epi deposition inserted post spacer formation to standard non-strained process
- Ease of implementation
Salicide Integration with SiGe

- NiSi compatible with SiGe (Co NOT compatible)
- NiSi has better narrow line scaling properties relative to CoSi$_2$ (IEDM 2002)

NiSi sheet resistance on SiGe (Ohms/square)

50 nm

IEDM 2003
Strained PMOS Performance

- Dramatic performance gain demonstrated for strained PMOS

\[ \text{Si}_{0.83}\text{Ge}_{0.17} : \]

- \( > 50\% \) \( I_{\text{DLIN}} \) Gain
- \( > 25\% \) \( I_{\text{DSAT}} \) Gain
Strained NMOS Transistor

- Developed a “Highly-Tensile” SiN capping film
- Uniaxially tensile strain induced in channel
- 10% $I_{DSAT}$ gain from tensile channel strain
Benefits of This Strain Approach

- Low cost (~2% process cost adder)
- Highly manufacturable way to introduce strain
- NMOS and PMOS performance optimized separately
- Mobility improvement maintained at high vertical fields
- Avoids cost, defect and integration issues associated with SiGe wafers
- Scalable to future generations
PMOS $I_{DSAT}$ vs $I_{OFF}$

$V_{DD} = 1.2V$
$T_{OX[physical]} = 1.2nm$

**High $V_{TH}$:**
$I_{OFF} = 40 \text{ nA/um}$
$I_{DSAT} = 0.7 \text{ mA/um}$

**Low $V_{TH}$:**
$I_{OFF} = 400 \text{ nA/um}$
$I_{DSAT} = 0.8 \text{ mA/um}$

$I_{OFF}$ (nA/µm) vs $I_{DSAT}$ (mA/µm)
NMOS $I_{DSAT}$ vs $I_{OFF}$

$V_{DD} = 1.2V$

$T_{OX}[physical] = 1.2nm$

**High $V_{TH}$:**
- $I_{OFF} = 40 \text{ nA/\mu m}$
- $I_{DSAT} = 1.26 \text{ mA/\mu m}$

**Low $V_{TH}$:**
- $I_{OFF} = 400 \text{ nA/\mu m}$
- $I_{DSAT} = 1.45 \text{ mA/\mu m}$

The graph shows a linear relationship between $I_{OFF}$ and $I_{DSAT}$ for different $V_{TH}$ conditions.
Sub-threshold Characteristics

Well controlled short channel effects
Subthreshold slope <100 mV/decade
Yield Challenge - SiGe Defects

Initial Development

After Focused Epi Defect Reduction Effort

Concern: Need for Selective SiGe Epi

Superb Epi Film Selectivity
Achieved Across 300mm Wafers
90nm defect reduction trend has been fastest ever
90nm yields are now at level needed for HVM
Summary

• A novel, highly manufacturable and cost-effective way to introduce strain is described with devices showing dramatic performance enhancement

• Highest drive currents reported to date at 90 nm node

• 90 nm defect reduction has been fastest ever and yields are now at level needed for high volume manufacturing

• Advanced CPU products are being ramped on this technology in two 300 mm wafer factories
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For further information on Intel's silicon technology, please visit the Silicon Showcase at

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